

Ultra-wide Bandwidth Inter-Chip Interconnects for Heterogeneous Millimeter-Wave and THz Circuits

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Abstract Heterogeneous chip-to-chip interconnects with low loss and ultra-wide bandwidths have been demonstrated. Coplanar waveguide-based interconnects between GaAs and Si die have been fabricated and characterized and the results compared to expectations from full-wave electromagnetic simulation. Broadband transmission characteristics were obtained, with insertion losses below 0.3 dB at 100 GHz and below 0.8 dB at frequencies up to 220 GHz demonstrated experimentally. The measured return loss exceeded 11.5 dB at all frequencies up to 220 GHz. The interconnects offer low latency, with a measured group delay of 0.69 ps. The measured results are in good agreement with full-wave simulations, indicating that the measured results do not suffer from significant impairments compared to theoretical predictions. The demonstrated interconnects offer an alternative to conventional approaches to millimeter-wave circuit and system integration, by enabling the compact realization of circuits in the microwave, millimeter-wave, sub-millimeter-wave, and THz frequency regimes in heterogeneous device technologies with very low chip-to-chip insertion loss.

Keywords Interconnects · Millimeter-wave circuits · Microwave circuits · Heterogeneous integration · Quilt Packaging

1 Introduction

Integrated millimeter-wave and terahertz systems are promising for a wide range of emerging applications, including imaging for security and avionics applications, as well as scientific and industrial applications such as material analysis, detection of subsurface defects, and

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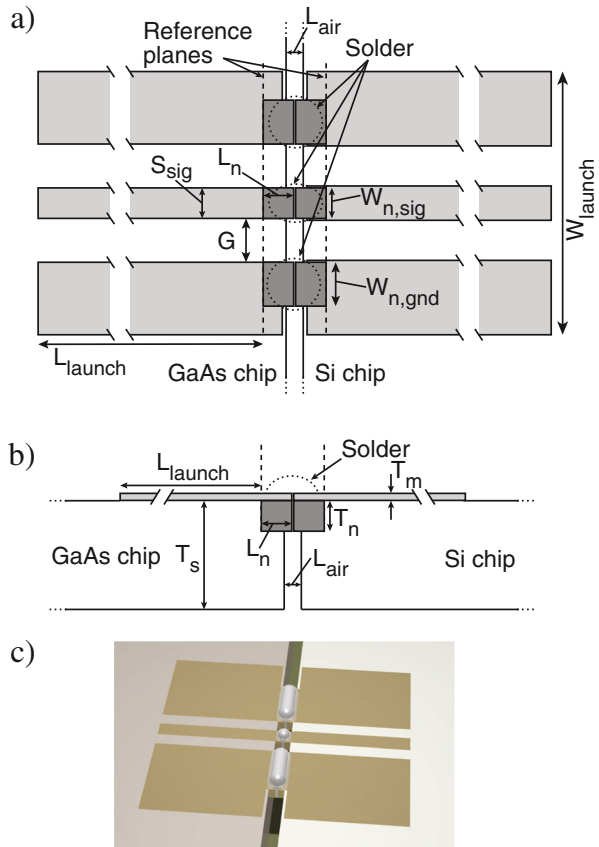
radiometry (see, e.g., [1–3]). While significant progress towards system-on-chip millimeter-wave and terahertz functionalities has been made, for high-performance applications, the ability to leverage specialized device technologies (e.g., compound semiconductor devices) and integrate them seamlessly with Si-based electronics in a heterogeneous system provides an attractive approach for achieving advanced functionality in a compact and efficient format. For these sorts of heterogeneous integrated systems, the ability to achieve wide-bandwidth, low-loss, low-latency interconnects between the constituent integrated circuits is essential for achieving sufficient system-level performance. Conventional approaches for system integration can impose limitations on performance (e.g., wirebonding and flip-chip interconnects impose electromagnetic discontinuities that limit bandwidth) or rely on precision machining (e.g., split-block assembly) that, although offering excellent performance, can be expensive and is typically limited to waveguide bands. In this letter, we report the performance of a compact, scalable, heterogeneous chip-to-chip interconnect between GaAs and Si die that offers extremely low insertion loss and latency from DC well into the millimeter-wave and sub-THz regime.

2 Interconnect Design and Fabrication

The chip-to-chip interconnects are based on coplanar on-chip waveguides that connect edge-to-edge between chips. Figure 1 shows a top view and schematic cross section of the interconnects, as well as a perspective view. Based on the “Quilt Packaging” approach, the interconnects consist of metallic nodules inlaid along the edge of each die that are connected to conventional first-layer metallization on each chip. The chips are placed adjacent to each other on a carrier and soldered together along the edges to form a continuous coplanar waveguide between chips. Thus, this technique provides a means to form a system-in-package consisting of multiple die fabricated in disparate and potentially incompatible process flows.

For the demonstration of heterogeneous integration reported here, the coplanar waveguide launchers on each chip were designed separately to provide a 50- Ω characteristic impedance and identical electrical length; to achieve this, the signal trace width (S_{sig}), gap (G), and launcher length (L_{launch}) were adjusted to compensate for the difference in dielectric constant between GaAs and Si. The nodules had the same overall geometry on each chip (width, length, and depth) but featured mating tabs and slots at their ends to facilitate accurate passive alignment [4, 5]. The geometric parameters (defined in Fig. 1) for the structures are given in Table 1. It should be noted that the parameter L_{air} accounts for the distance that the nodules from each chip protrude and bridge the space between the chips; this includes both the overhang from each nodule as well as any solder present between chips. For the designs reported here, the nominal L_{air} (i.e., without any solder between interconnected nodules) is 10 μm ; we estimate that 5 μm of solder is present in these structures, leading to a total L_{air} of ~ 15 μm in the fabricated structures. Due to the similar dielectric constant of Si and GaAs, as shown in Table 1, the launcher geometries on the Si and GaAs chips reported here are similar, leading to only modest mismatch between modes at the interface between chips. For interconnects between chips with disparate dielectric constants for which the transmission line geometries are quite different (e.g., quartz and Si), lithographically defined tapers in the launcher and nodule geometries can be used for compensation to maintain insertion loss and return loss [6] at the expense of reduced bandwidth. Similarly, if chips of different thicknesses are to be joined, the surfaces of the two chips must be coplanar to within the thickness of the

Fig. 1 Schematic top view, cross-section view, and perspective view (to scale) of heterogeneous chip-to-chip interconnect



nodes ($T_n = 20 \mu\text{m}$ for the nodes used here). This level of assembly tolerance is well within typical specifications for package machining and die thinning processes. Experimentally, we observe little effect on interconnect performance through G-band for small ($\sim 10 \mu\text{m}$) deviations in alignment or planarity [7]. In addition, with modest geometric scaling, reduction in linewidth roughness, and improvements in the solder process (e.g., use of eutectic reflow), simulation studies have suggested that bandwidths exceeding 1 THz should be possible with this approach [8].

Table 1 Design parameters for launchers and nodes

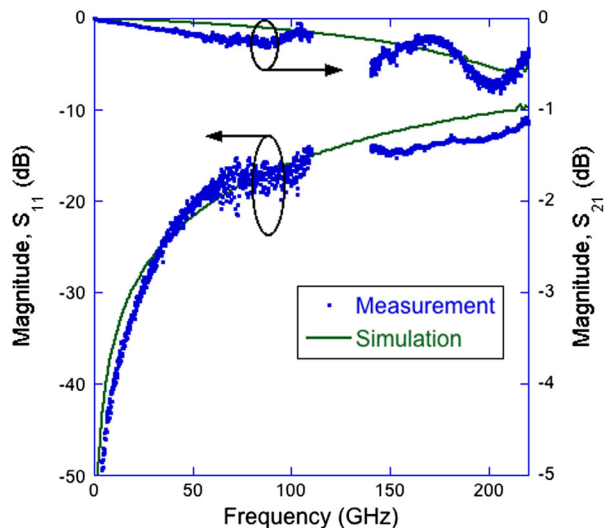
Design parameter	Dimension (μm)	Design parameter	Dimension (μm)
$S_{\text{sig,GaAs}}$	30	$S_{\text{sig,Si}}$	32
G_{GaAs}	26	G_{Si}	25
$L_{\text{launch,GaAs}}$	250	$L_{\text{launch,Si}}$	259
$W_{n,\text{sig}}$	30	$W_{n,\text{gnd}}$	100
W_{launch}	420	T_n	20
L_n	25	T_s	100
L_{air}	10–15	T_m	0.4

Fabrication processes for high-resistivity Si [9] and semi-insulating GaAs [10] die have been reported previously; the key steps are the formation of the inlaid nodules (using inductively coupled reactive ion etching (ICP-RIE), plating, and chemical–mechanical polishing), the formation of partial-thickness die separation streets using ICP-RIE (for the die reported here, the separation etch was $\sim 150\text{ }\mu\text{m}$ deep, while the wafer thickness was $500\text{ }\mu\text{m}$), and thinning of the die using backside grinding to a final thickness of $100\text{ }\mu\text{m}$. This final thinning step also singulates the die. For the structures reported here, the soldering was performed by using solder paste (Kester R276), applied to the nodules using pin transfer, followed by a reflow step at $270\text{ }^{\circ}\text{C}$ for 30 s in laboratory air using commercial die-attach equipment. The fabrication and assembly is based on well-established processes that provide the potential for high throughput and fully automated assembly.

3 Characterization and Interconnect Performance

Interconnects with the dimensions described above were fabricated, and also simulated numerically using Ansys HFSS [10]. Figure 2 shows the measured and simulated insertion loss and return loss for these structures. Measurements were made using on-wafer probing from 0.1 to 110 GHz , and from 140 to 220 GHz in two bands. To suppress higher-order modes in the launcher structures, the chips were placed on carbon-impregnated microwave absorbers on the chuck of a probe station. One hundred-micrometer pitch ground-signal-ground Cascade Infinity on-wafer probes were used for the measurements. To improve measurement and calibration repeatability, the probe station was equipped with high-resolution ($1\text{-}\mu\text{m}$ resolution, $3\text{-}\mu\text{m}$ accuracy) digital run-out gauges on the probe positioners for both vertical and lateral travel. This allows the operator to accurately set both the relative probe-to-probe spacing as well as the over-travel during probing. A two-tier calibration was used, with off-wafer impedance standards used for the first tier, followed by on-chip through-reflect-line (TRL) calibration in the second tier to set the s-parameter reference planes at the junction between the nodules and the launchers, as shown schematically in Fig. 1. The on-chip calibration standards

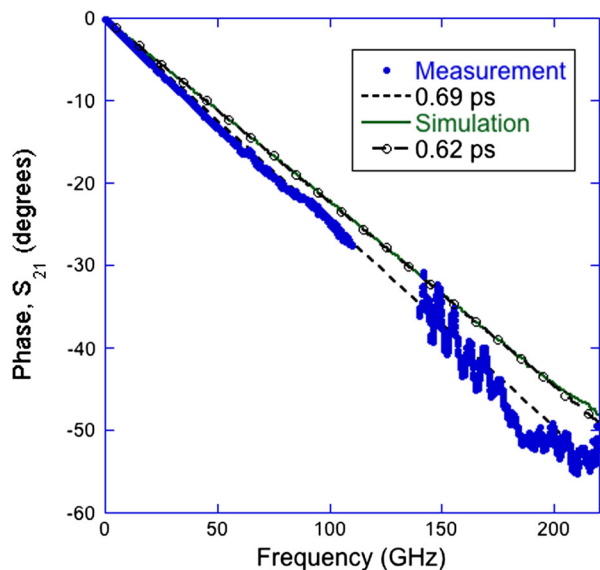
Fig. 2 Measured and simulated s-parameters for GaAs-Si heterogeneous chip-to-chip interconnects. Good agreement between measurement and simulation is obtained, with a measured insertion loss below 0.8 dB achieved at up to 220 GHz . The loss through 110 GHz is below 0.3 dB . The measured return loss exceeds 11.5 dB at all measured frequencies



(offset opens, through and delay lines) were fabricated simultaneously and in the same process flow with the launchers and interconnects. For the HFSS simulations, the interconnect structures (including the launchers) were simulated, along with the on-chip calibration structures; these simulation results were then post-processed using the TRL calibration algorithm so that the reference planes in the measurements are identical to those in the simulations. In the HFSS simulations, loss in the dielectric substrates (GaAs and Si) was included, as were conductive losses in the metallization (Ti/Au, 0.4 μm thick) and radiative losses. For consistency with the experimental configuration, the simulations also included a 3-mm-thick carbon-impregnated AlN absorber underneath the chips (modeled as a dielectric constant of 9 and loss tangent of 0.3).

As can be seen in Fig. 2, a measured insertion loss of less than 0.8 dB from 0.1 to 220 GHz has been obtained, with a measured return loss greater than 11.5 dB over the full frequency range. The measured insertion loss tracks the simulation projections closely, with no more 0.2-dB deviation over the full frequency range. Likewise, the return loss also agrees well, with the most significant deviation being approximately 0.75–2-dB lower return loss at G band from the measurements than that predicted by simulation. The roughly sinusoidal deviation between the measured and simulated insertion loss at G band (140–220 GHz) is attributable to minor imperfections in the second-tier on-wafer calibration. To be conservative, we quote here the highest measured insertion loss. Simulation suggests that an insertion loss of 0.53 dB at 220 GHz should be expected if the calibration artifacts are eliminated. For frequencies up to 110 GHz, worst-case insertion loss is 0.25 dB (at 87.5 GHz in Fig. 2), with a return loss better than 16 dB. These measured results compare favorably with other integration approaches, including flip-chip integration and split-block waveguide-MMIC transitions. Flip-chip integration has been demonstrated with insertion loss of 0.6 dB to 100 GHz at 15-dB return loss (see e.g., [11]), but typically requires high-impedance compensation sections that increase area and reduce bandwidth [12]. For split-block waveguide transitions, transition losses of approximately 1 dB have been achieved (see e.g., [13]), corresponding to a chip-to-chip loss of ~ 2 dB and return losses of ~ 10 dB. Waveguide approaches are limited to the bandwidth of the host waveguide. Recently, a J-band (220–260) transition exhibiting <1 -dB insertion loss at

Fig. 3 Measured and simulated insertion phase delay as a function of frequency, along with best-fit lines for delay



220 GHz and return loss exceeding 10 dB has also been reported, based on silicon micromachining processes and cavity-backed coplanar waveguides [14]. To the authors' knowledge, the Quilt Packaging-based edge-interconnect structure reported here represents the lowest insertion loss at these millimeter-wave and sub-THz frequencies for heterogeneous chip-to-chip integration, while maintaining return losses above 10 dB, and offering ultra-wide bandwidths (from DC through millimeter-wave frequencies).

The latency and group delay of the interconnects were also assessed. Figure 3 shows the measured and simulated insertion phase delay for the GaAs-Si interconnects, along with best-fit lines to constant delay. As can be seen, the simulations indicate that an almost dispersionless delay of 0.62 ps matches the results well, while the measurements result in a slightly larger delay of approximately 0.69 ps. This 70-fs deviation may arise in part from the deviation in geometric parameter L_{air} between the simulations and the structure that was characterized experimentally. For the simulations, no solder was included between the nodules (they were assumed to abut directly), with a total L_{air} of 10 μm (note however that the total distance between s-parameter reference planes is appreciably larger than 10 μm , leading to the larger total delay). Experimentally, however, we routinely observe that solder penetrates between the nodules during reflow, resulting in a slightly increased L_{air} value due to the finite thickness of the solder. This solder thickness is typically on the order of 5 μm . We estimate that this effect likely accounts for around one quarter of the observed deviation in phase; the rest is believed to be due to imprecision in probe positioning during measurement. An error in probe position of 4 μm would be sufficient to induce this degree of phase discrepancy (due to the larger dielectric constant of the substrates compared to air); this level of error is consistent with our probe placement repeatability. The nearly linear-phase characteristics and extremely short latency (measured at <0.7 ps) suggest that these interconnects are promising for ultra-wide bandwidth interconnects with low distortion.

4 Conclusion

Heterogeneous integration between GaAs and Si die using the Quilt Packaging paradigm has been reported for the first time. Extremely low insertion losses below 0.3 and 0.8 dB have been obtained at frequencies up to 110 and 220 GHz, respectively, in good agreement with predictions from numerical electromagnetic simulations. The return loss of the chip-to-chip interconnects is also very good, with measured values exceeding 11.5 dB over the full frequency range from 0.1 to 220 GHz. The demonstrated heterogeneous interconnection approach appears promising for enabling the compact, cost-effective realization of future highly integrated microwave, millimeter-wave, sub-millimeter-wave, and THz circuits and systems based on heterogeneous device technologies.

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